



VoTeR Center

UConn Voting Technology Research Center

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Design for Intrinsically Nonvolatile Memory
Compatible With AccuVote Optical Scan Memory Cards
Technical Report

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Abstract

One current AVOS memory card requires maintenance because the batteries discharge.

A memory card using an intrinsically non-volatile RAM has been designed to be compatible with the AVOS; its design is given herein. Moreover, a prototype version of this card, has been designed and tested. This card has a compatible interface, but is dimensionally different. Proper functioning was demonstrated by writing it with one AVOS, and reading it with test software that reads and stores card content.

The intrinsically non-volatile, surface mount design, with electrostatic discharge protection, appears to be possible, and affordable, compared with an existing design. A switch to a new design along these lines is suggested.

Chapter 1

Introduction

Some electronic voting machines have used nonvolatile memory cards, having an internal battery for the purpose of providing nonvolatility of the data. Battery-supplied cards have experienced problems [2]. Given the difficulties experienced with batteries, and the apparent ease of designing and manufacturing a memory card that did not rely on batteries, it seemed desirable to do so.

This report describes an intrinsically nonvolatile design with electrostatic discharge protection.

The organization of the report is a description of the design, followed by a justification for consideration of electrostatic discharge protection, which shows the importance of identification of the memory card / system unit boundary as a proprietary external interface, warranting test procedures and a specification for the independent testing authorities (ITAs).

A design for the electrically/electronically and mechanically compatible card is presented. Appendices show close up views of the schematics and printed circuits.

Chapter 2

Non-volatile Memory Card Design

2.1 Prior work on Memory Design

Memory card design has electrical, logical, mechanical and thermal aspects. The electrical aspects are greatly simplified by the use of standard components designed for interoperability. Electrical noise on the power connections is filtered using the common practice: with bypass capacitors and such resistance as the circuit boards traces provide. Logical design includes meeting the timing requirements. GANTT charts, invented for the design of transistor circuits, and made broadly popular in the generalization of their application to include time management of human enterprises, continue to be useful in the analysis of logic circuit timing. The mechanical constraints were met by choosing surface mount components.

Standard wide temperature range parts were used.

2.2 Design

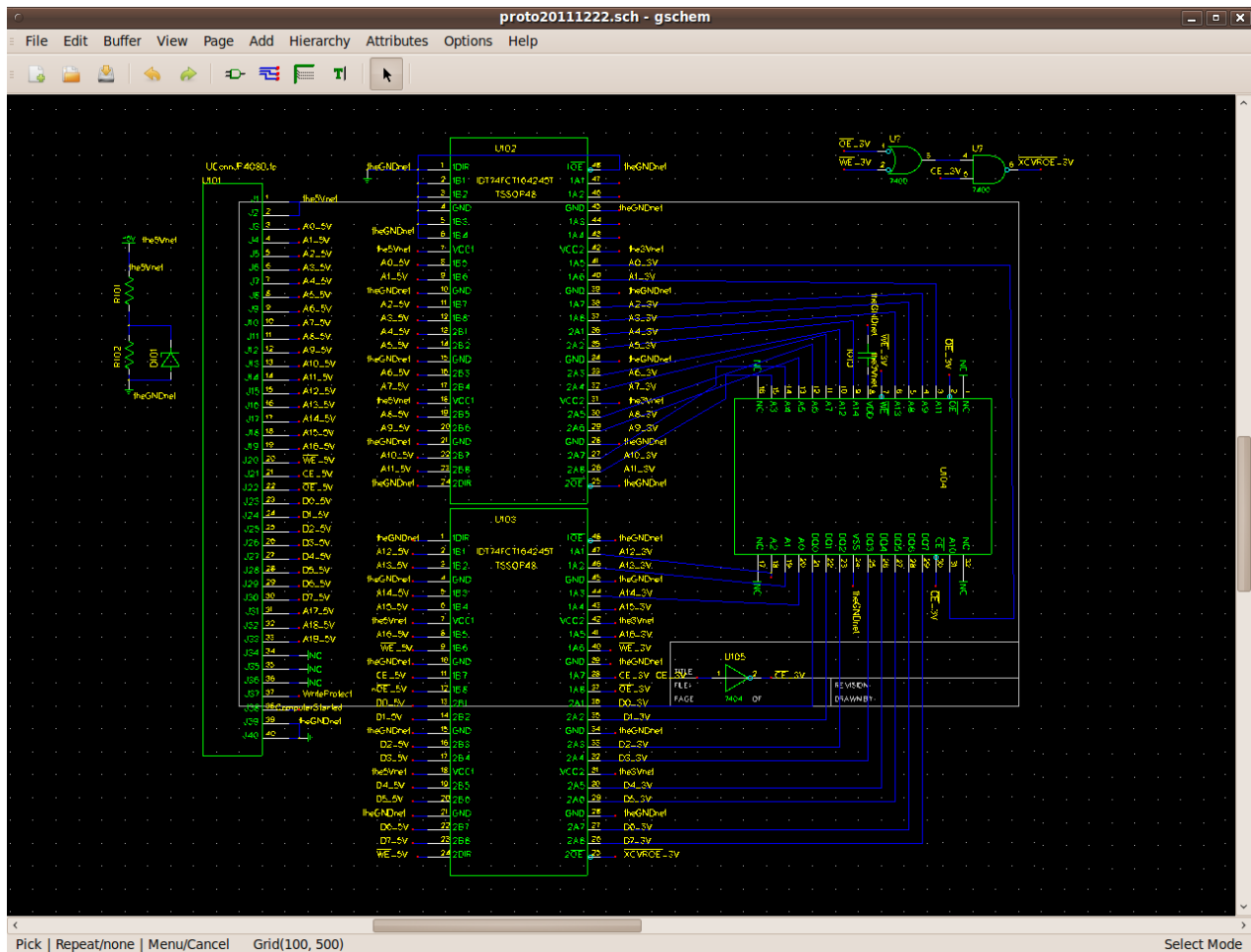
The design of the memory card has electrical, mechanical (prominently size), and thermal considerations. The nonvolatile RAM (the FRAM by RAMTRON) is used. At the RAMTRON website (<http://ramtron.com/about-us/what-is-f-ram.aspx>, viewed 2011-12-27) one finds “Like F-RAM, ROM (read only memory) is a nonvolatile memory that does not lose its data content when power is removed. Newer generation ROM, like EEPROM (electrically erasable programmable read only memory) and flash memory, can be erased and re-programmed multiple times, but they require high voltage and write very slowly. ROM-based technologies eventually wear out (in as little as 100,000 cycles), making them unsuitable for high-endurance industrial applications.

F-RAM has 10,000 times greater endurance and 3,000 times less power consumption than a typical serial EEPROM device, and nearly 500 times the write speed”.

Transceivers are used for considerations of voltage levels, current drive and electrostatic protection.

For its nonvolatile properties and compatibility, the FM28V020 chip by RAMTRON International was selected as the appropriate memory device. The voltage levels appropriate to this device are the more modern 0-3V rather than the 0-5V range. A voltage translation circuit designed for the purpose of interfacing the 0-5V domain with the 0-3V domain is used to provide interoperability of these two sets of signals. The IDT74FCT164245T transceiver, from Integrated Device Technology (www.idt.com, viewed 2011-12-27) is used for this function. As this voltage interoperability finds itself useful often at interfaces between circuits, the benefit of a certain amount of electrostatic protection, namely ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0), (see http://www.datasheetcatalog.org/datasheet/idt/74FCT164245T_Datasheet.pdf, viewed 2011-12-27) is also provided by the IDT74FCT164245T transceiver.

The design also includes development of the voltage supply needed by the 3V parts, using a Zener diode.



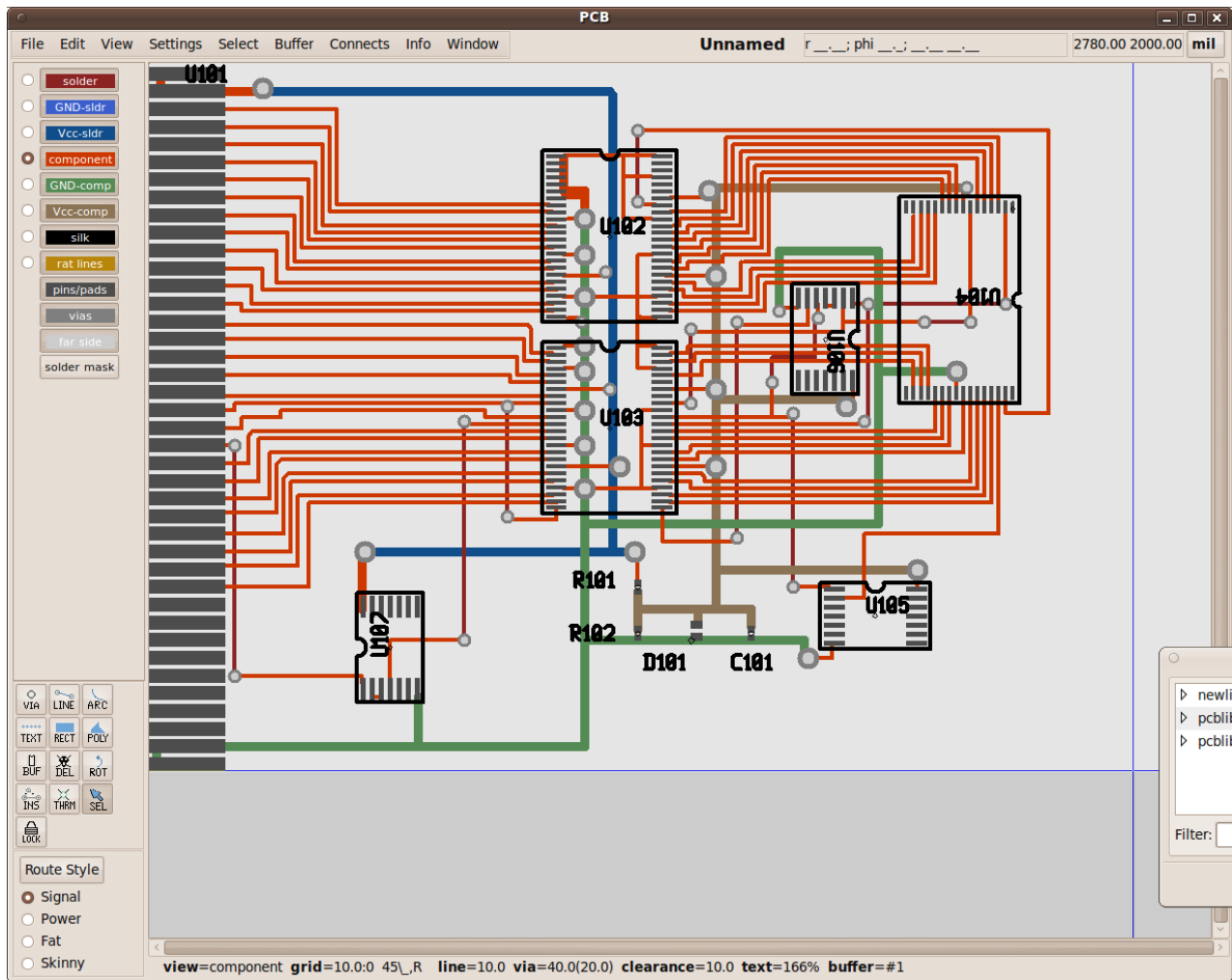


Figure 2.2: Memory Card – Printed Circuit Card Layout. Note the 2 inch dimension, vertical in the figure, corresponding to the width of the memory card.

2.3 Testing

The prototype card was tested by programming it with an AVOS and GEMS configuration. The card was then carried (without external power) to another AVOS where it was used as if in an election. Then the card was carried, again without external power, to a device which was used to extract (“dump”) the content of the card. The data were correct. The experimental board worked but was unreliable, probably due to construction – but it provides a proof-of-concept for the FRAM design.

Chapter 3

Recommendations

In the setting that the electronic voting equipment has components parts, to be handled separately by the election officials, it is appropriate that the officials be informed of proper handling procedures, to avoid unnecessary damage to the component parts, and thus delay the end of life of the component parts.

Thus, should a deficit of such instruction be available from the vendor, it is not inappropriate that an advisory agency, such as VoTeR Center, offer some suggestions for maintaining the component parts in good order.

The memory design proposed herein has, for chips directly connected to its interface, component parts specified to be resistant to electrostatic discharge. In the interest of maintaining the State's stock of cards, the following recommendations are made:

3.1 Electrostatic Discharge Protection

The specification sheet [3] for an SRAM considered gives maximum and minimum values for the voltages that may appear on the SRAM pins (These are called absolute maximum ratings, and stress beyond these can be expected to damage the chip.). The values are -0.5 V to 7V compared to the voltage of the ground pin.

It would be very inexpensive, easy and prudent to carry the memory cards from the current inventory in antistatic packaging. The current plastic covers bear a recycling seal identifying the material as polyvinyl chloride (PVC), of which it is possible to obtain an antistatic variety, see, for example, http://www.boedeker.com/pvc300_p.htm.

According to [1, p. 3], "In a typical work environment a charge of about $0.6\mu C$ can be induced on a body capacitance of 150 pF, leading to electrostatic potentials of 4000 volts or greater. Any contact by the charged human body with a grounded object such as an IC pin an result in a discharge for about 100 nanoseconds with peak currents in the ampere range. The energy associated with this discharge could mean failure to electronic devices and components.", and goes on to cite McAteer [4, p. 41-48] "Many semiconductor devices can be damaged even at a few hundred volts but the damage is too weak to be detected easily, resulting is what is known as *walking wounded* or *latency effect*". ESD goes on to say [1, p. 4]that "Electrical Overstress (EOS) events can occur due to electrical transients at the board level or the system level. . . . EOS is increasingly considered to be a major issue demanding more attention as it becomes a significant failure mode in the IC industry." ESD goes on to say [1, p. 4]that "The damage due to human handling can be reduced by the proper use of wrist straps for grounding the accumulated charges and shielded bags for carrying the individual [parts]". ESD goes on to say [1, p. 4]that "Even with good protection circuits, devices are not necessarily immune to ESD once they are on the circuit boards. Other forms of ESD from the charged boards are possible. Thus ESD precautions are important during system assembly as well."

The removal and introduction of the memory card in current use, with respect to the AccuVote box is the same as assembly, for the purposes of this discussion, namely the need to avoid ESD damage.

Comparing the absolute maximum voltage on the Hynix SRAM, of 7 volts, with the electrostatic discharge expected from a person walking across a floor with a synthetic carpet in relative humidity of 20%, which is 35 kilovolts according to the table [1, p. 10], reprinted from [5]. ESD goes on to say [1, p. 9] that the currents and energy dissipated are large enough to cause damage, due to the very small dimension of the semiconductor structures. Since ESD was written (1995), the reduction in device dimensions has been significant which only exacerbates the problem. On pages 10 and 11, ESD [1] describes the human body model, machine model and charged device model (CDM). For the case of electronic voting technology with removable sensitive parts like the memory card, the human body model applies when a person walks to a card, for example, over a carpet, and touches the card. The charged device model applies when a person carries a card, for example, while walking across a floor, and then puts the card down.

To avoid these events that accumulate charge, making the discharge of current through an IC more probable, electoral officials handling the memory card would be equipped with a grounded anti-static mat, which they would touch after walking (or locomoting in any fashion) to the equipment. Having touched the mat, the official would then attach a grounded wrist strap to themselves. Then the memory card could be removed and should be placed directly into an antistatic bag, which should have been in contact with the antistatic mat. Once the card is sealed within the bag, the bag can be carried from place to place. The bag should not be opened until the bag is in contact with a static mat.

Static mats and wrist strap assemblies can be obtained for around \$100, less in quantity. A means of grounding this antistatic equipment, such as wiring it to the plumbing, or to the third wire in a grounded three-wire electrical power socket, must be used. The socket, if it is used as the source of ground, should be checked, as with a household 3-wire electrical socket tester.

ESD states [1, p. 18-19] that “One of the issues raised with CDM type damage is that of cold healing, whereby the damage anneals with time at room temperature”, citing Verhaege, [7]. ESD [1, p. 18-19] goes on to say that “It is not certain whether such effects can lead to a latent reliability hazard, but the possibility must certainly be considered when evaluating the effect of CDM damage.”

The significant possibility of having induced a latent reliability hazard suggests that consideration whether the existing stock of memory cards might be so afflicted, and whether a test for this status might be warranted, if it could be performed in a non-destructive manner.

ESD states [1, p. 21-22] that “the result (of ESD) can be an increase in the leakage current either at the stressed pin or between other pins, especially between the supply pins.”

What this means for our memory card in current use is, in the event a memory card RAM was damaged at the address pins (which are exposed on the card’s interface, and are perhaps more vulnerable than the equally exposed data pins) the damage could manifest as an increased demand upon the battery.

A means of testing the reliability of the memory card should be provided. The current means has been shown to be inadequate[2].

A memory design not requiring battery backup can be readily obtained using ferroelectric RAM, such as are available from Ramtron International, of Colorado Springs, Colorado.

An additional design approach would be the use of a more flexible circuit board material, such as that sold by allflex, of Northfield, MN, and described at <http://www.allflexinc.com/bene.shtml> (viewed 2011-12-27).

For the existing memory cards, a means of reducing the likelihood of flexion that might induce intermittent loss of battery power might be helpful.

A means of testing the existing stock of memory cards for bad solder joints would be desirable. Of course it is desirable to perform this test through the interface, which is a significant restriction. There is a principle called a time domain reflectometry, that measures the length of conductive paths, by means of detecting the time delay of reflections of energy.[6] If the energy used in the measurement is low enough that it would not damage the circuit, then a signature of a well soldered board could be compared with the results for a board with known bad solder joints, and the sensitivity of the discrimination between the two situations might be used as an assurance that the board would continue to function after being inserted and removed from the

electronic voting equipment.

A means of inserting and extracting the memory card, such as a fixture that holds the card by its edges, and applies force in a repeatable fashion, and in a location apart from the battery, whose contacts are likely to be unreliable, might be recommended. The industry term for these devices is card ejectors. It is conceivable that the existing cards could be fitted with ejectors.

A non-destructive means of testing whether a memory card, as delivered to a district, is reliable to support an election might include a measurement of the effectiveness of the conductors leading from the edge connector inwards to the circuits on the board. Time domain reflectometry is such a method.

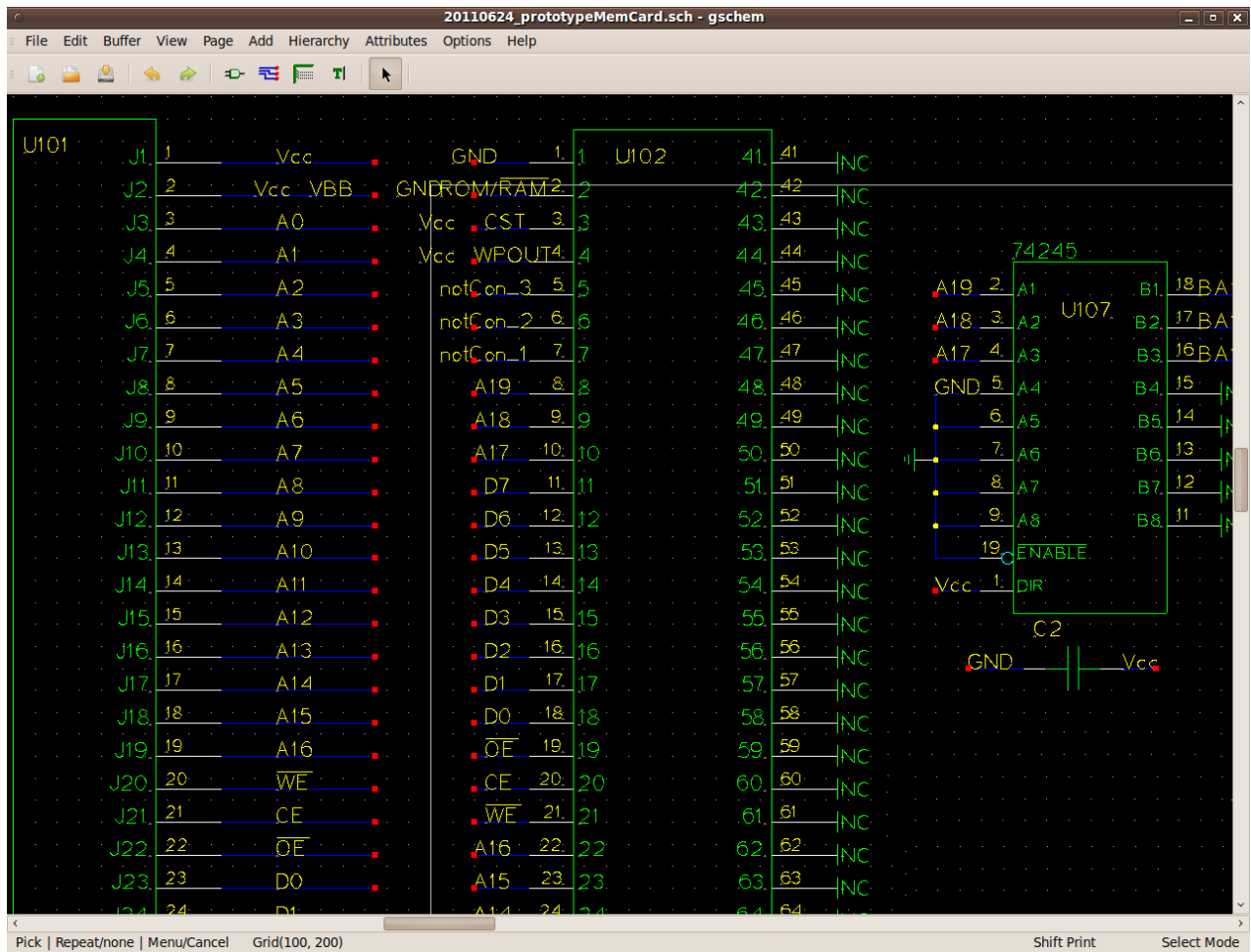
A means of evaluating the utility of measures such as these to protect the memory cards is desirable.

Bibliography

- [1] A. Amerasekera and C. Duvvury. *ESD in Silicon Integrated Circuits*. Wiley, 1995.
- [2] T. Antonyan, N. Nicolaou, A. A. Shvartsman, and T. Smith. Determining the causes of accuvote optical scan voting terminal memory card failures. *online proceedings of EVT/WOTE 2010*, 2010. Also available as http://www.usenix.org/events/evtwote10/tech/full_papers/Antonyan.pdf and <http://voter.engr.uconn.edu/voter/reports/>.
- [3] hynix. Hy628100b series, 4 2001.
- [4] O. J. McAteer, R. E. Twist, and R. C. Walker. Latent esd failures. *Proc. 4th EOS/ESD Symposium*, 1982.
- [5] R. Y. Moss. Caution—electrostatic discharge at work. *IEEE Trans. Comp. Hyb. and Man., CHMT-5*, page=512-515, 1982.
- [6] D. Smolyansky. *Electronic Package Fault Isolation Using TDR*, pages 289–302. ASM International, 2004.
- [7] K. Verhaege, G. Groesenken, and H. Maes. Influence of tester, test method and device type on cdm testing. *Proc. 16th EOS/ESD Symposium*, 1994.

Chapter 4

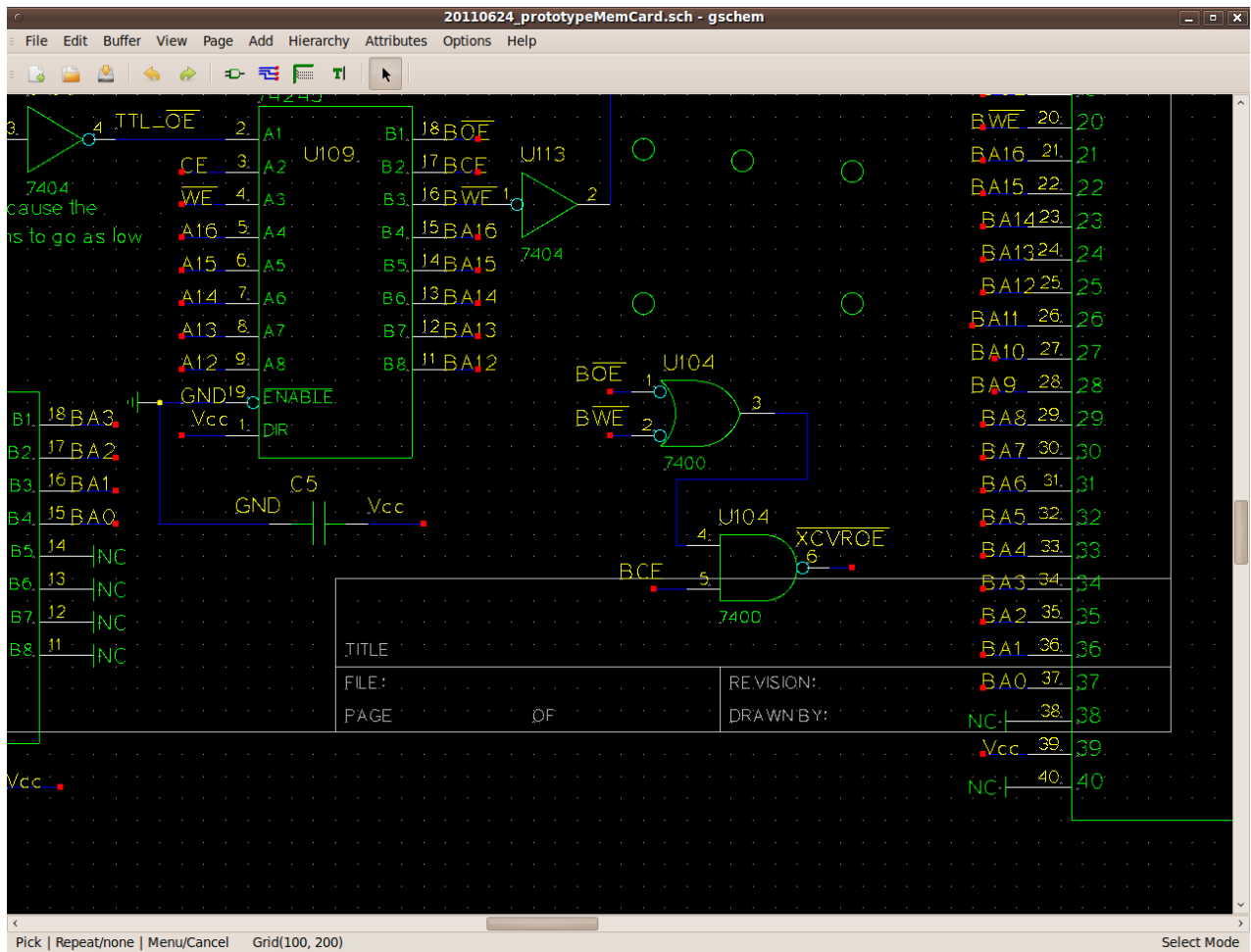
Schematics Closeups, Memory Card for Prototyping



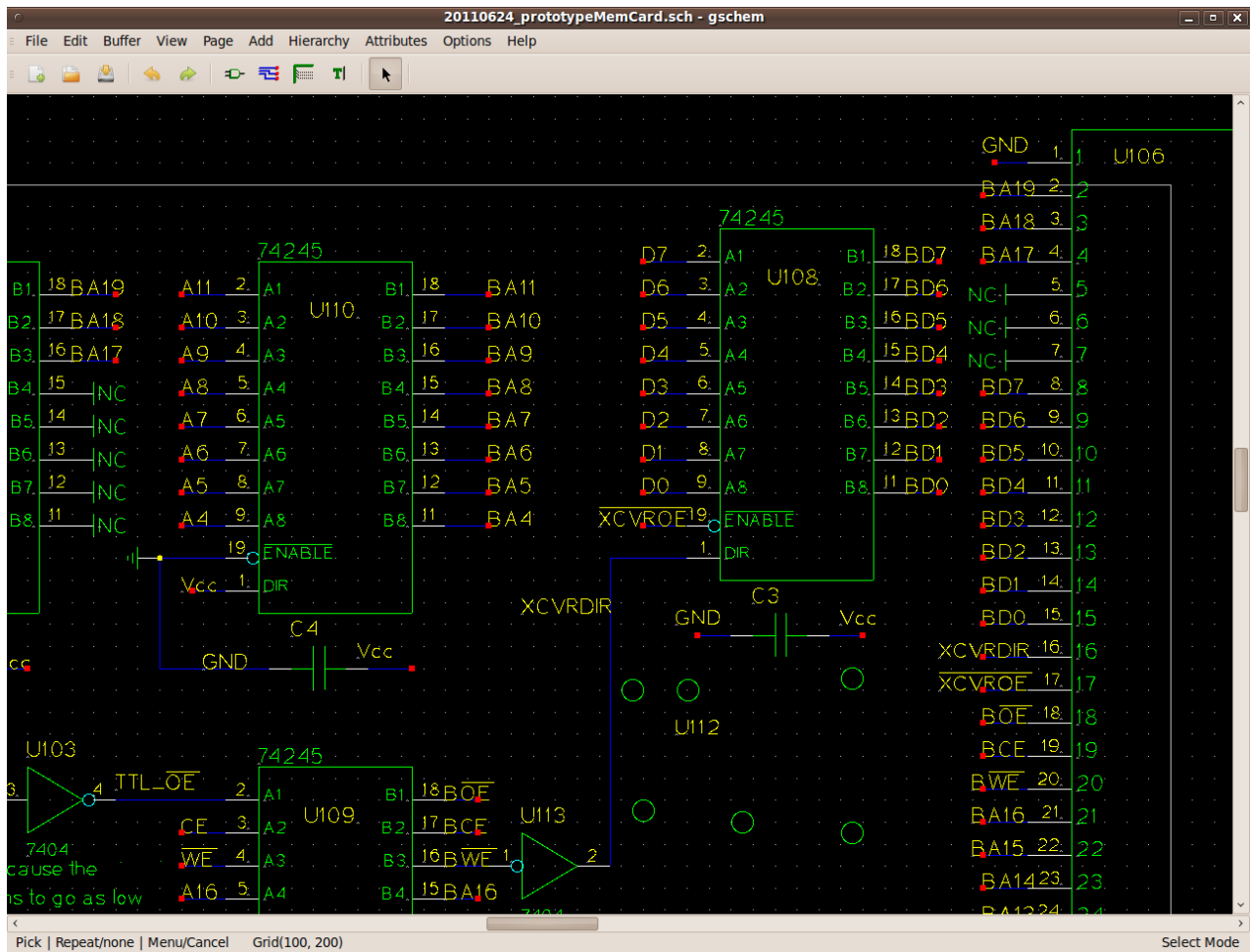
Upper left corner of schematic of memory card for prototyping.



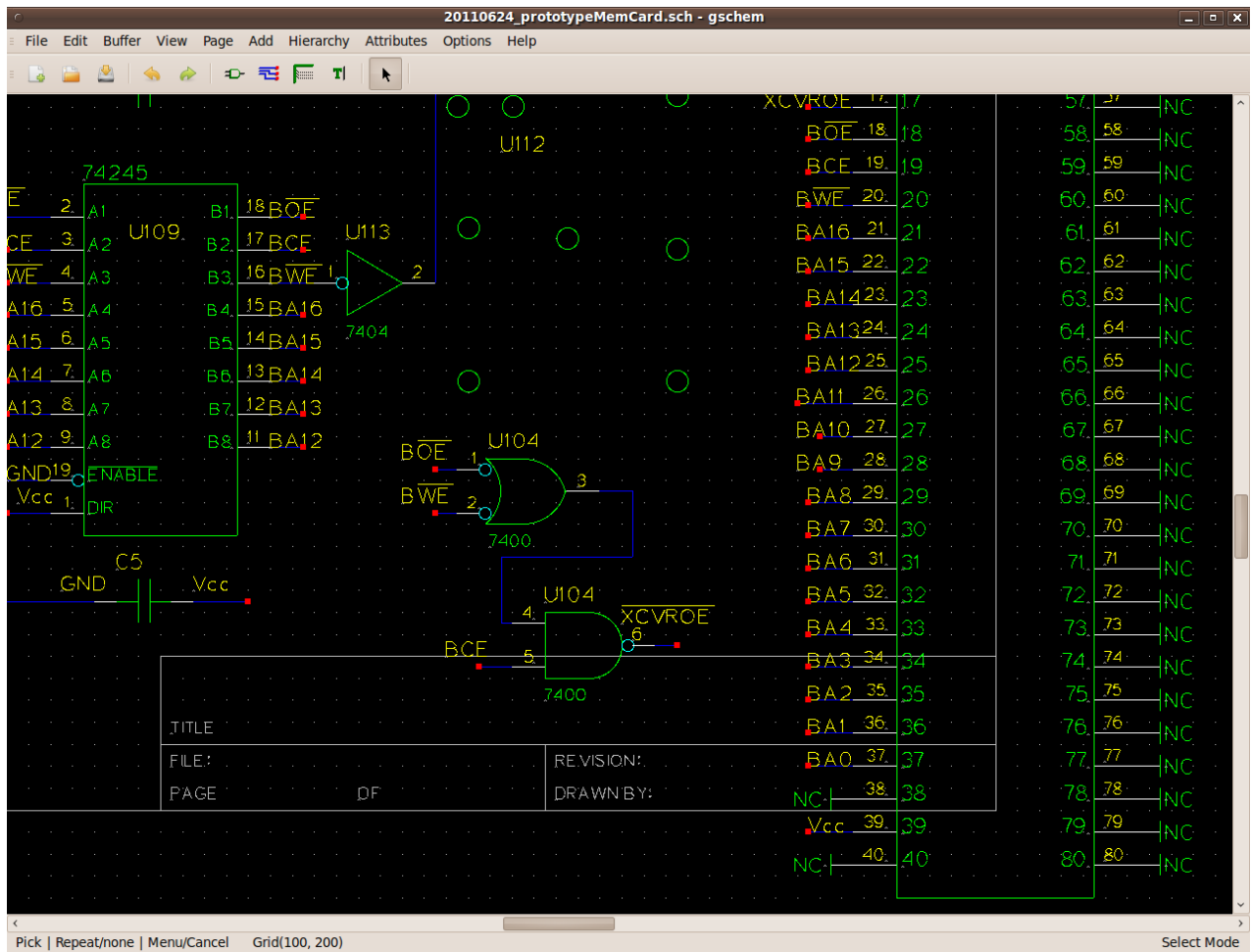
Lower left corner of schematic of memory card for prototyping.



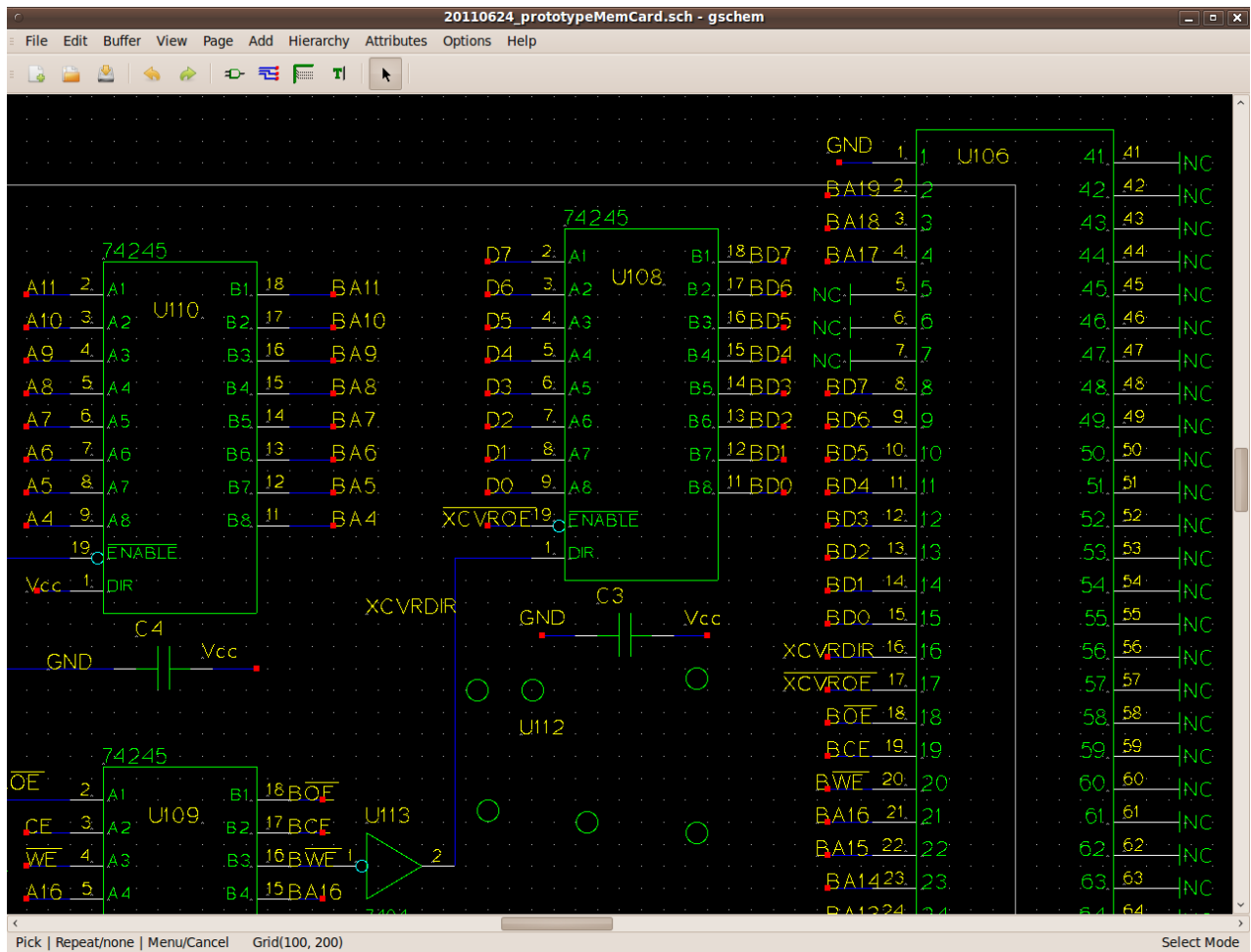
Lower middle section of schematic of memory card for prototyping.



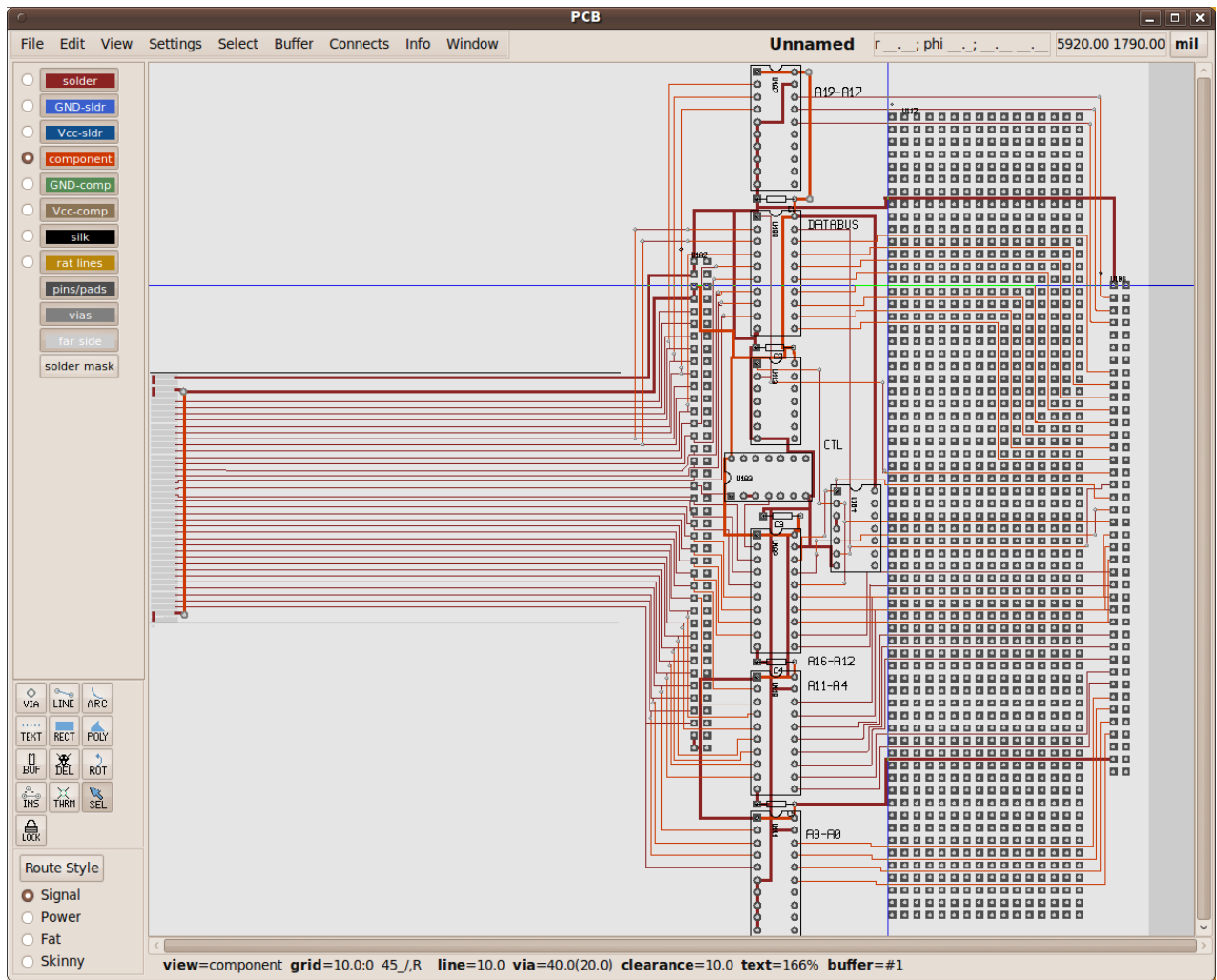
Upper middle section of schematic of memory card for prototyping.



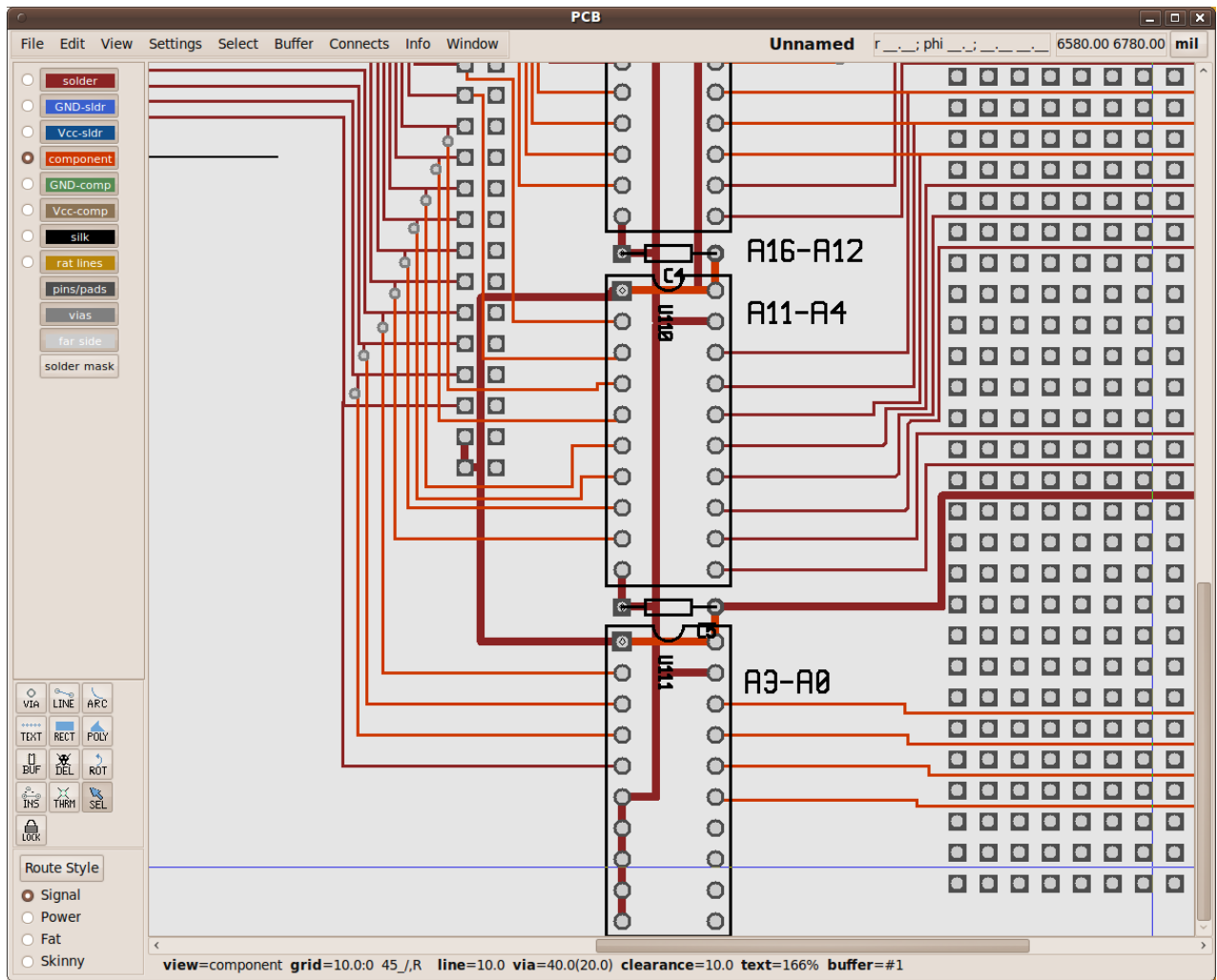
Lower right section of schematic of memory card for prototyping.



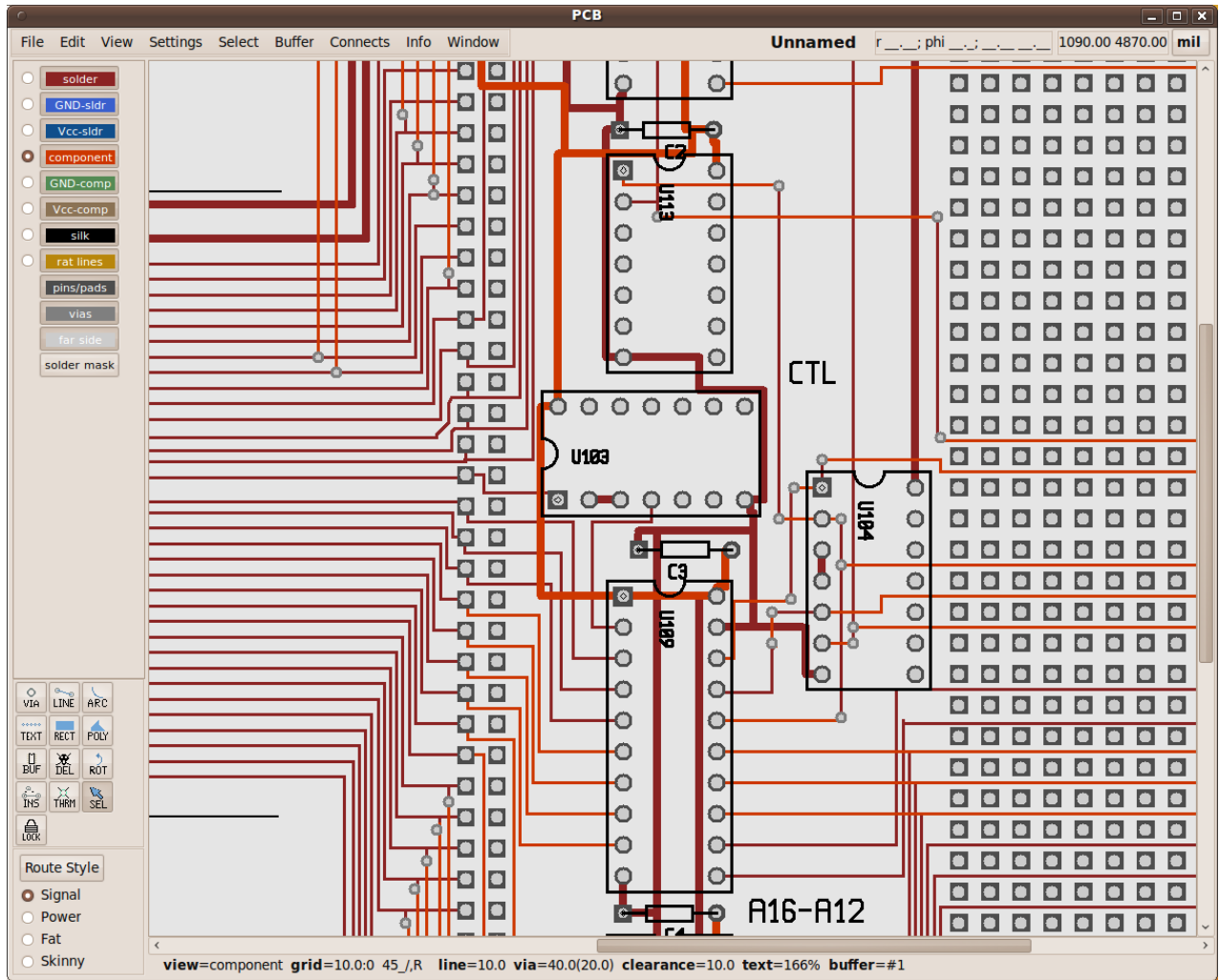
Upper right section of schematic of memory card for prototyping.



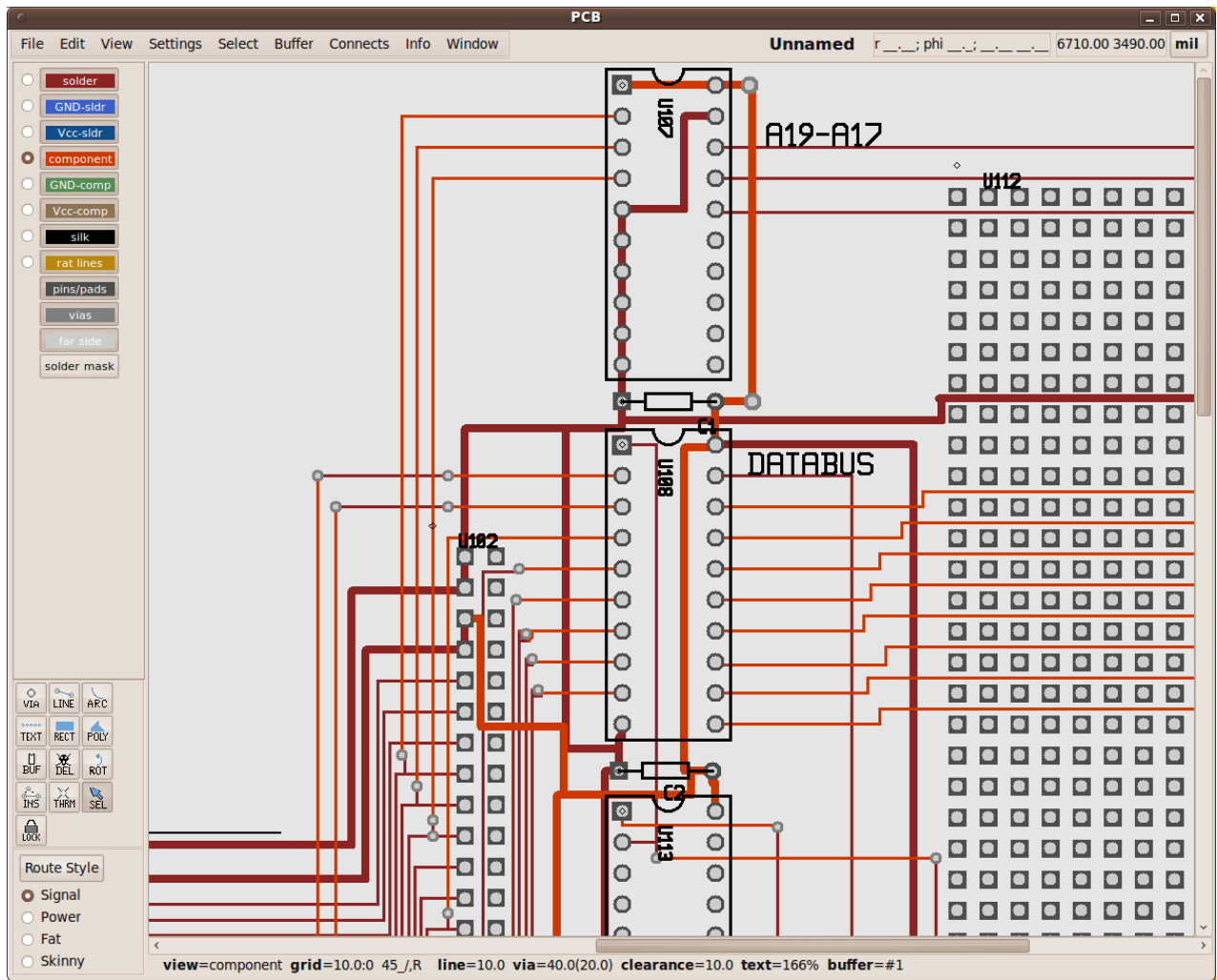
Printed circuit for prototyping: printed wiring whole board.



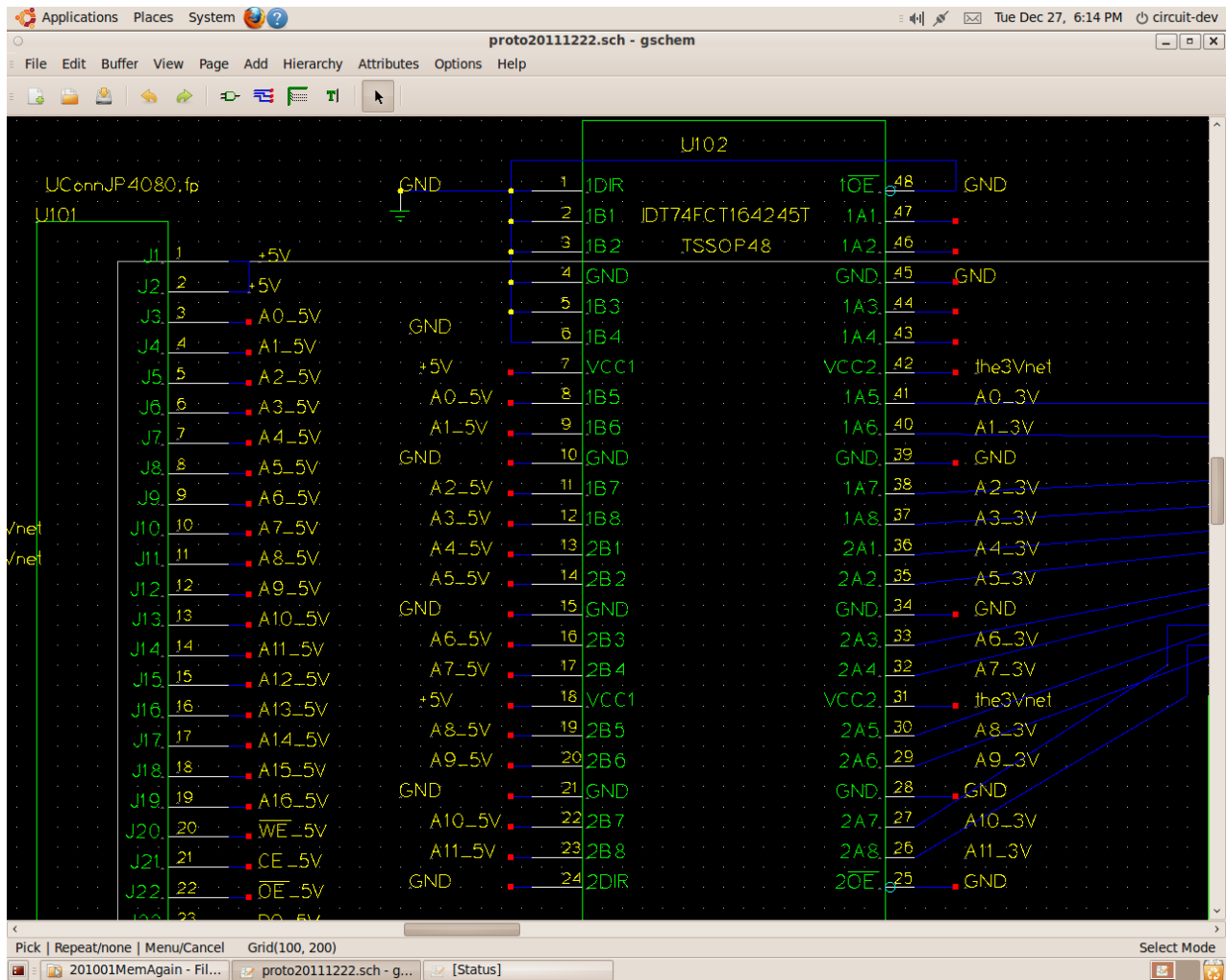
Printed circuit for prototyping: printed wiring in bottom middle



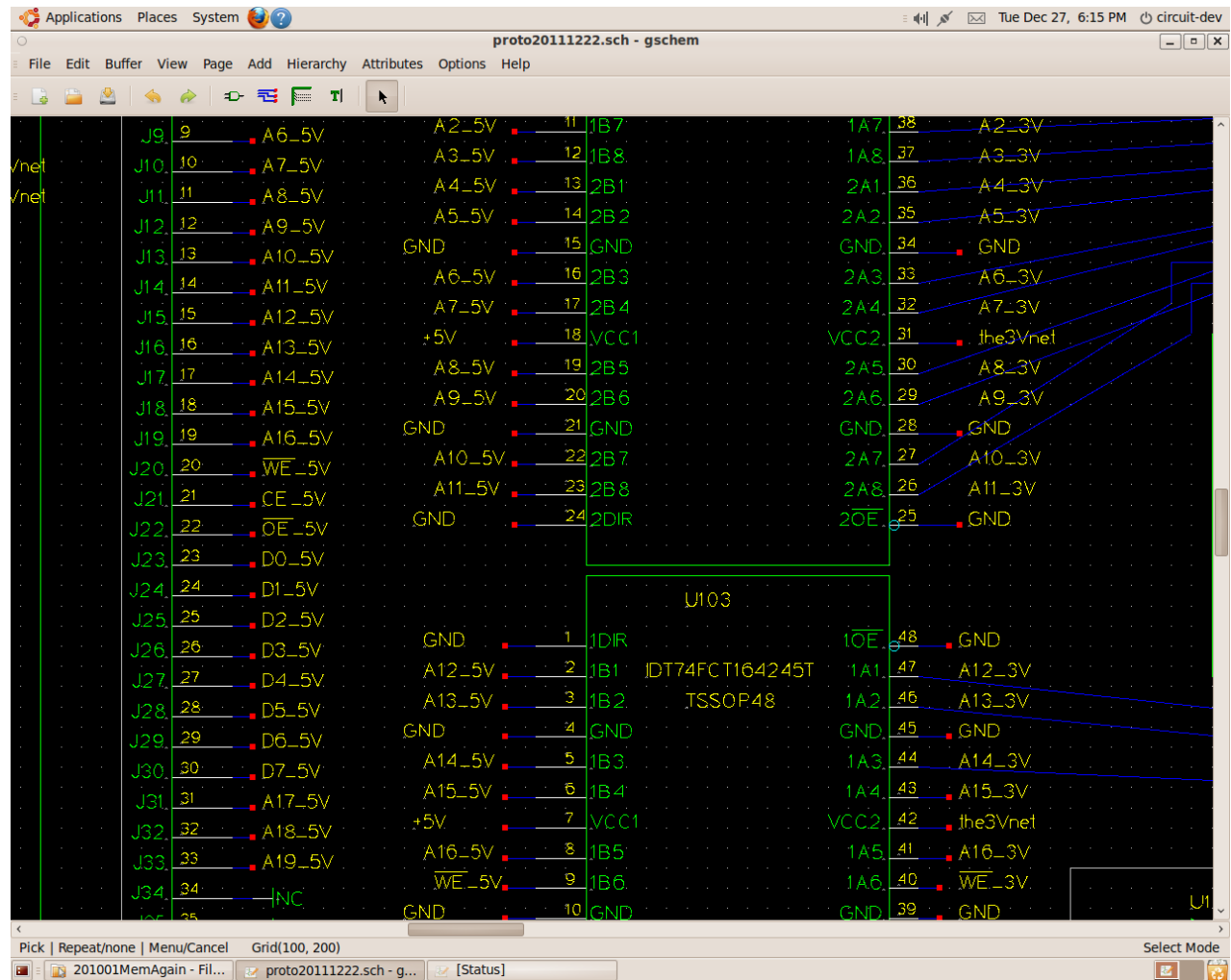
Printed circuit for prototyping: printed wiring in center.



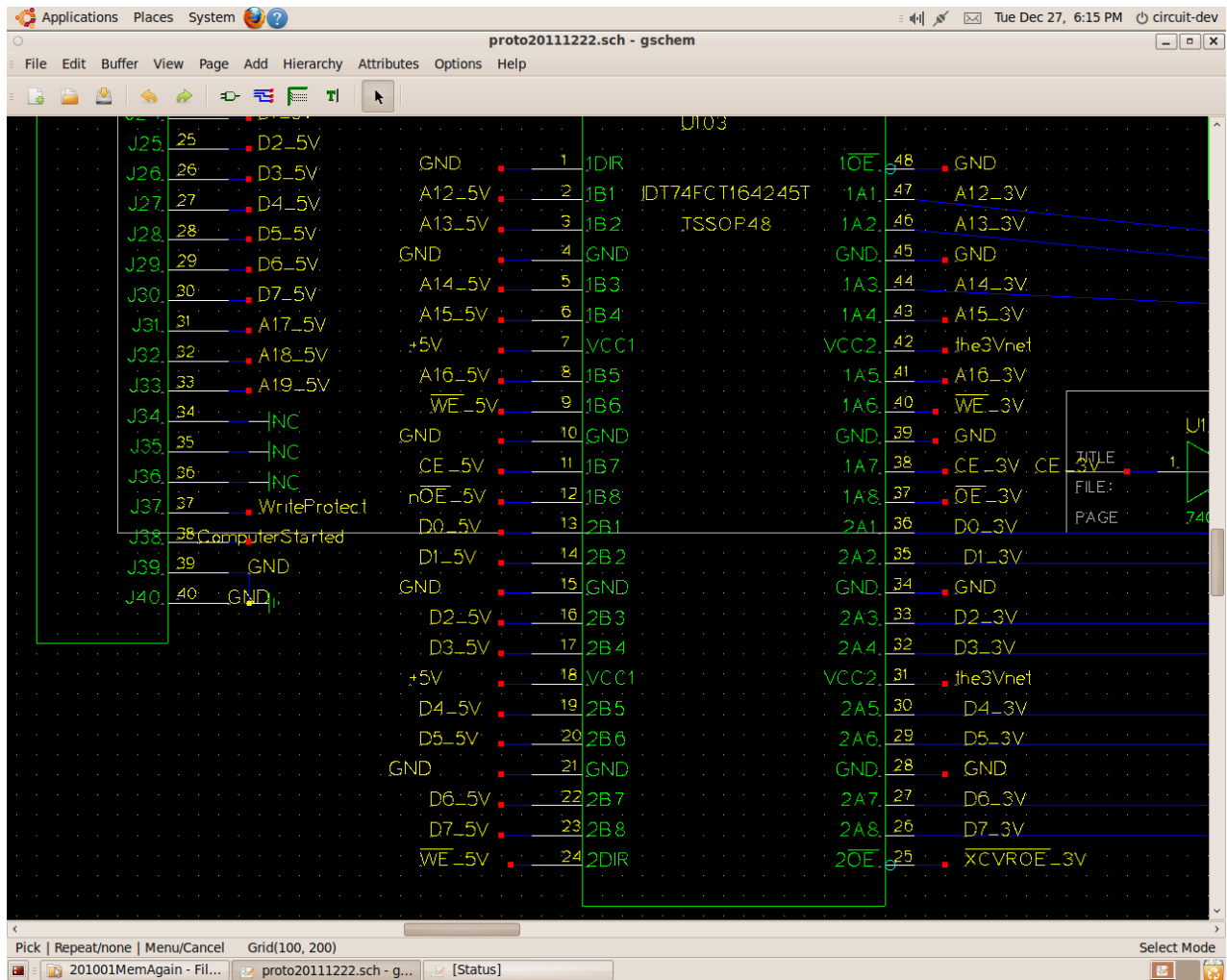
Printed circuit for prototyping: printed wiring in top middle.



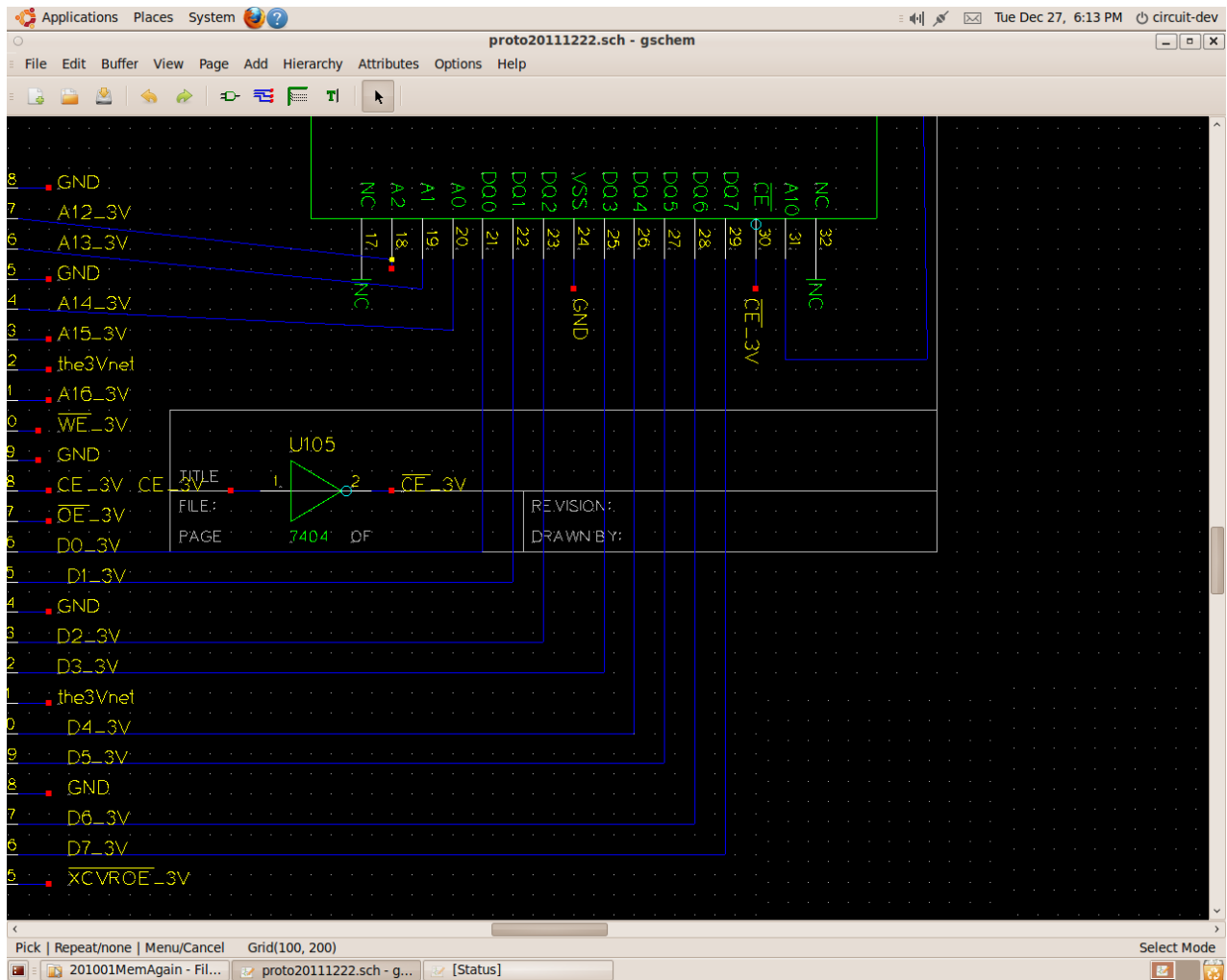
Printed circuit for memory: schematic in top middle.



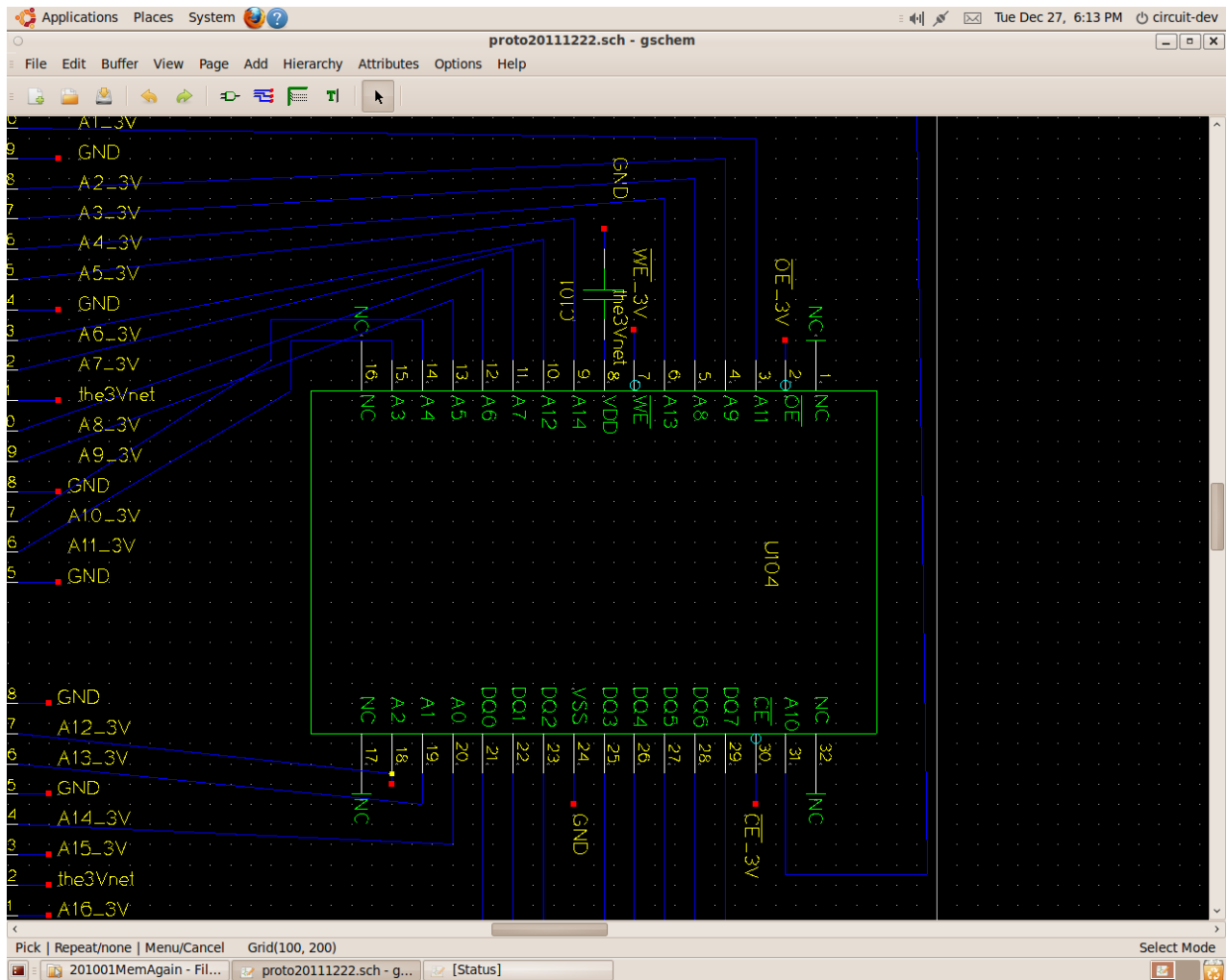
Printed circuit for memory: schematic in middle.



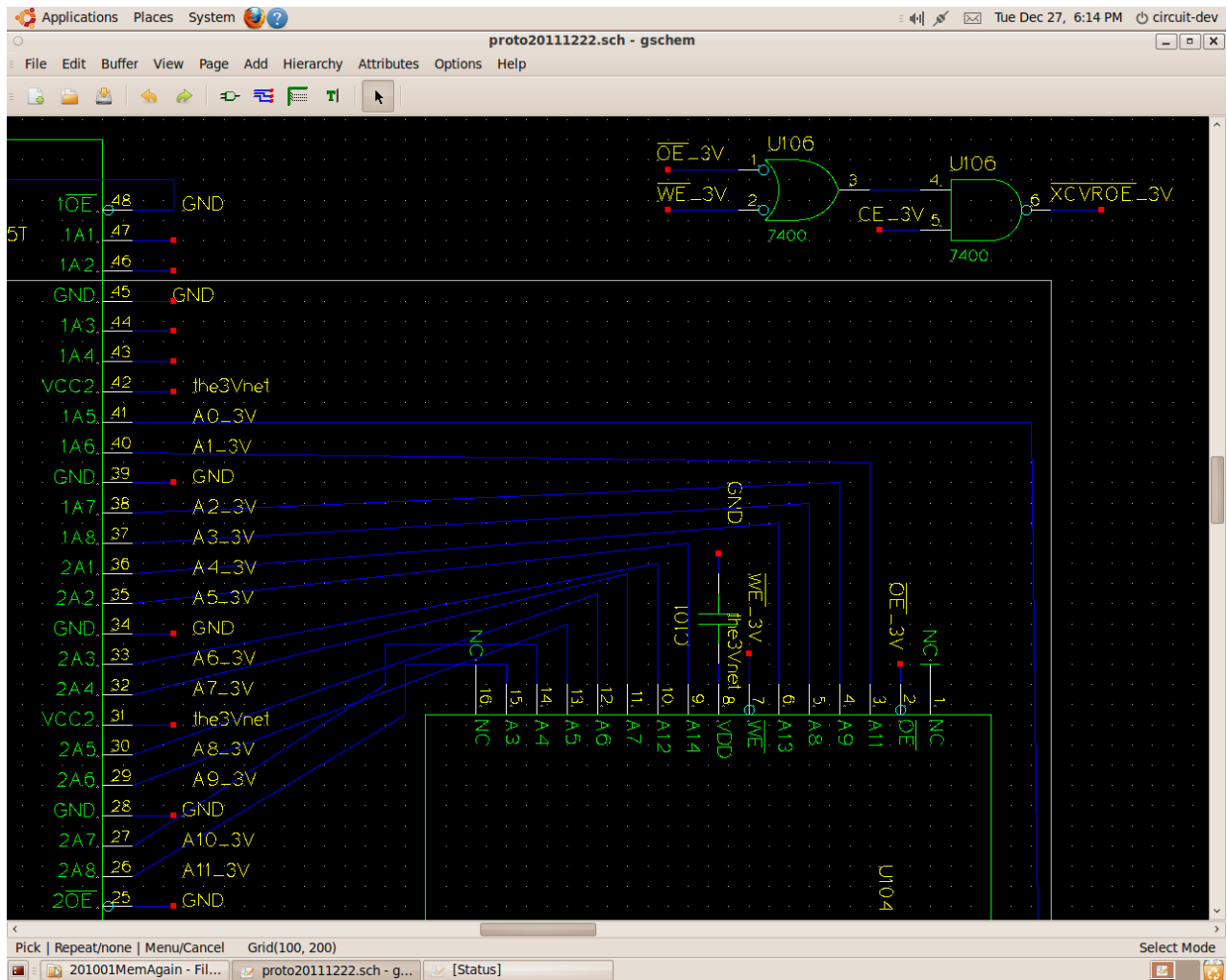
Printed circuit for memory: schematic in lower middle.



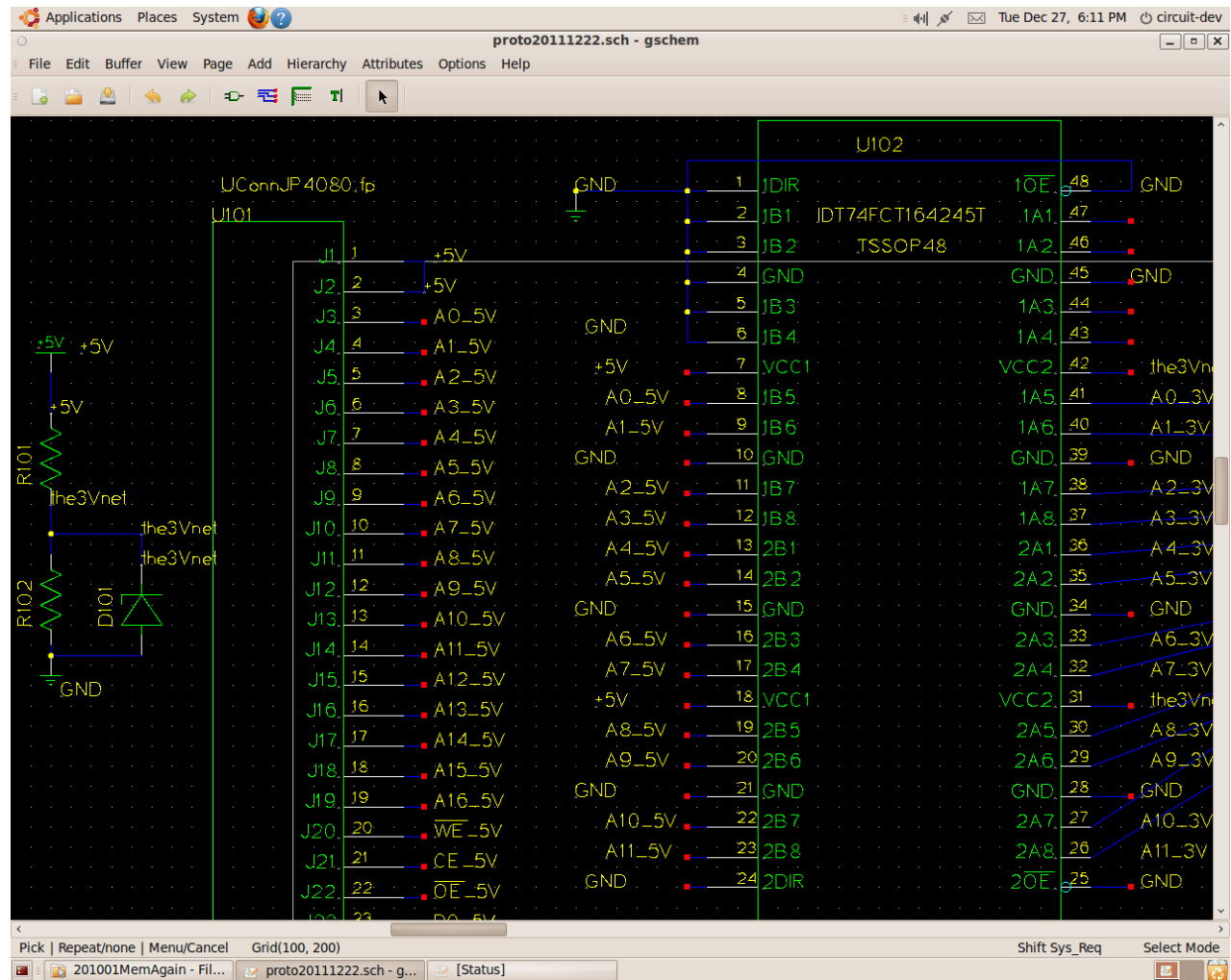
Printed circuit for memory: schematic in lower right.



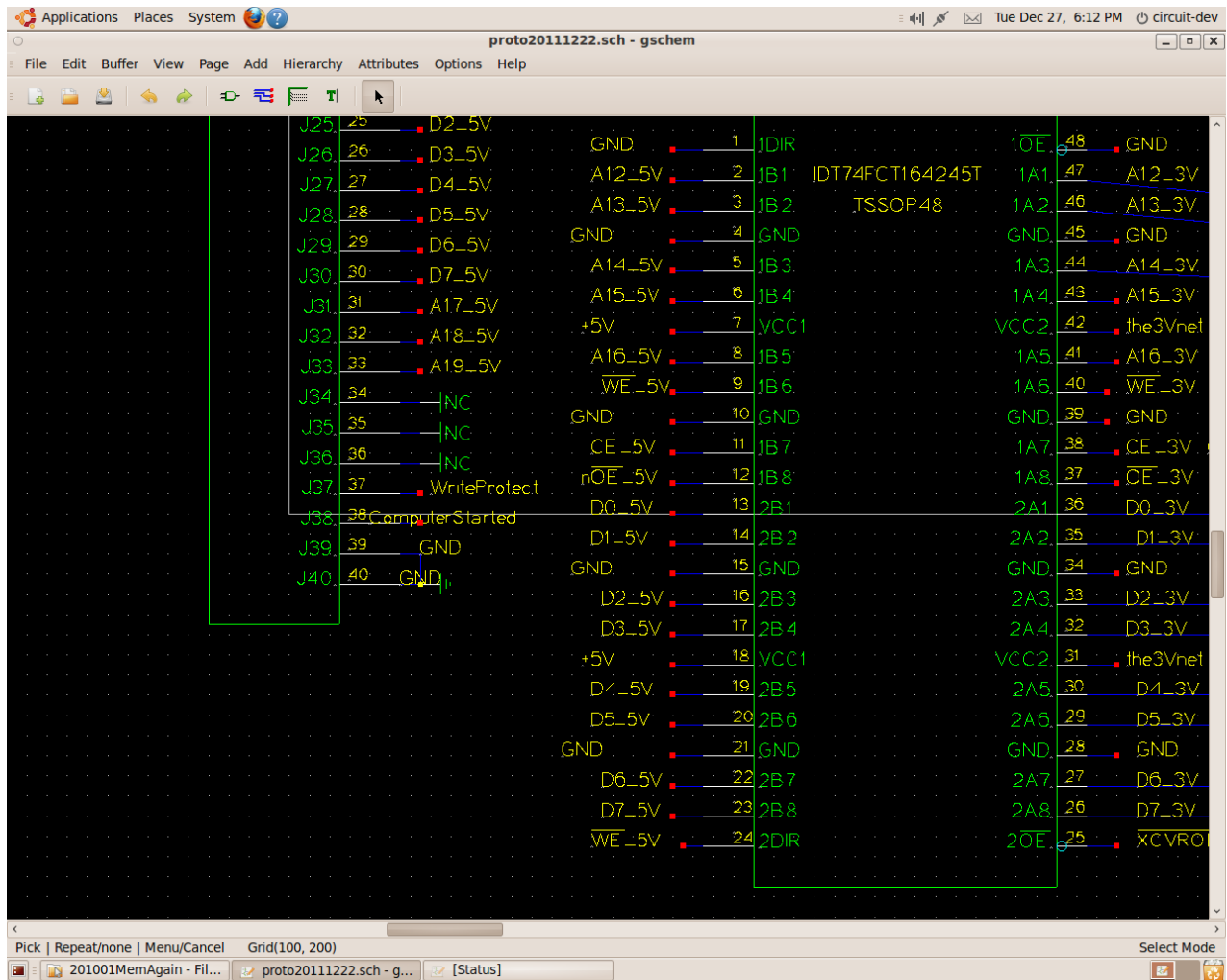
Printed circuit for memory: schematic in right middle.



Printed circuit for memory: schematic in upper right.



Printed circuit for memory: schematic in upper left.



Printed circuit for memory: schematic in lower left.